23 19

CH 30. (New) The processor of claim 26 wherein the result is returned to a result register which is a different register than either the first or second operand registers.

REMARKS

Applicants thank the Examiner for the courtesy extended to Applicants and Applicants' representative during an interview on January 16, 2003. During the interview, Applicants presented proposed claim amendments and proposed new claims which are substantially the same as presented in the present amendment. Applicants discussed the invention with the Examiner and illustrated that the specification provides support for the amended and newly added claims. For example, Applicants directed the Examiner's attention to at least Figure 8 and the relevant discussion of Figure 8 on pages 9-11 to illustrate support for claiming a system for performing a group-convolve instruction comprising means for multiplying a selection of symbols determined by the indices of the symbols and adding a plurality of selected products so as to produce a plurality of result symbols. As another example, Applicants also directed the Examiner's attention to at least Figure 3 and the relevant discussion of Figures 1-4 on pages 5-6 to illustrate support for claiming a group-multiply instruction of floating point operands and a defined bit width that is dynamically variable. Applicants also pointed out that at least each of Figures 1-6 illustrate multiplying in parallel. It is Applicants' understanding, based on the discussions in the interview, that the Examiner was satisfied with Applicants' discussion of support for the amended and newly presented claims.

Applicants also pointed out, that original claims 8 and 12 are generic claims to a floating point operation (presented in amended claim 10 and new claim 16, and amended claim 14 and

C

new claim 17, dependent on claims 8 and 12, respectively) and to a fixed-point arithmetic operation (presented in original claims 9 and 13, dependent on claims 8 and 12 respectively). During the course of the interview, the Examiner indicated that new claims 22 and 26 would be more consistent with original claims 8 and 12 if the result was recited to be capable of being represented by a bit width equal to said defined bit width of said operands. The Examiner did not suggest that such addition was required by the prior art or for the patentability of claims 22 and 26 in any manner. In order to expedite the Examination process, Applicants have presented new claims 22 and 26 which recite floating point products being capable of being represented by a bit width which is equal to the defined bit width of the operands. It is Applicants' understanding, based on the interview, that the Examiner will enter and examine the newly presented claims.

I. Introduction

The Specification stands objected to because the filed specification does not contain an adequate top margin.

Claims 8-30 are pending in the above application.

Claims 16-30 are newly added.

Claims 8-15 stand rejected under 35 U.S.C. § 101 under the doctrine of obviousness-type double patenting.

Claims 10 and 14 stand rejected under 35 U.S.C. § 112¶2 as being indefinite for being duplicates of claims 9 and 13, respectively.

II. Amendments

A. Substitute Specification

A substitute specification is being provided to overcome the informality of the margin as pointed out by the Examiner. The priority claim has also been updated to reflect issuance of U.S. Serial No. 08/516,036 as U.S. Patent No. 5,742,840 and the issuance of U.S. Serial No. 08/516,036 as U.S. Patent No. 5,742,840, and also to clarify language that § 120 priority is being claimed on U.S. Serial No. 08/516,036, filed Aug. 16, 1995, now U.S. Patent No. 5,742,840. A substitute Declaration has also been provided to prevent any ambiguity regarding the priority claim. No new matter has been added to the specification.

In reviewing the specification, Applicants have also discovered various typographical and text placement/formatting errors in the pseudo code presented on pages 15-16 of the original application. It is believed that these errors were introduced by the text editor used to prepare the application from the provisional application. Applicants note that the correct pseudo code was correctly provided in the provisional application upon which the present application is based. The corrected pseudo code is provided in the substitute specification. One of skill in the art would readily identify the corrected pseudo code as intended to be recited by the specification and to be within the possession of the Applicants at the time of filing the above application. Particularly, the written text of the disclosure makes the errors and the correction of those errors readily apparent to those of skill in the art. For example, the correct recitations for the "G.MUL" and the "G.U.MUL" instructions are provided to one of skill in the art at least by the discussions set forth on page 5, lines 22-27 of the original disclosure. Likewise, the correct recitation for the "G.MUL.SUM" instruction is provided to one of skill in the art at least in the discussion set forth on page 7, line 24 through page 8, line 3 of the original disclosure. Further, the correct recitation

for the "G.CONVOLVE" instruction is provided to one of skill in the art at least in the discussion set forth on page 9, line 26 through page 10, line 7. As an Applicant is not required to present computer code in describing their invention (see, MPEP 2106.01 Written Description, "[t]he function of the description requirement is to ensure that the inventor had possession of ... the specific subject matter ... how the specification accomplishes that is not material"), the pseudo code was provided simply as an easy reference to illustrate that which is described in the text of the disclosure. The corrections to the pseudo code simply bring the recitations in the pseudo code in conformance with the text of the disclosure and/or eliminate obvious errors therefrom.

A mark-up copy of the substitute specification is also attached. No new matter has been added to the substitute specification.

B. Claims

Claims 10 and 14 have been amended such that they are not duplicates of claims 9 and 13, respectively. Accordingly, the rejection on claims 10 and 14 under 35 U.S.C. § 112¶2 is believed to be overcome.

Claim 15 has also been amended to more clearly set forth that which Applicants regard as the invention recited therein.

Claims 16-30 are newly added.

No new matter has been added by the amendments to the claims or the specification.

III. Double Patenting Rejection

Claims 8-15 stand rejected under 35 U.S.C. § 101 under the doctrine of obviousness-type double patenting as being unpatentable over claims 1-7 of U.S. Patent No. 5,953,241.

A terminal disclaimer is being filed with this response, and is believed to be sufficient to overcome the obviousness-type double patenting rejection of claims 8-15. No further response is believed to be necessary.

IV. Conclusion

Having fully and completely responded to the Office Action, Applicants submit that all of the claims are now in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,
MCDERMOTT, WILL & EMERY

Lawrence T. Cullen
Registration No. 44,489

600 13th Street, N.W.
Washington, DC 20005-3096
(202)756-8000 MEF:MWE
Facsimile: (202)756-8087
Date: February 4, 2003

APPENDIX B

IN THE SPECIFICATION:

Please replace the Specification with the Substitute Specification attached in Appendix A1, a mark-up copy of the Substitute Specification is attached in Appendix A2.

IN THE CLAIMS:

Please amend claims 10, 14 and 15 and add new claims 16-30 as follows:

10. (Amended) The method for performing a group-multiply-and-sum instruction according to claim [8] 16, wherein the instruction comprises a [fixed-point] floating-point arithmetic operation.

14. (Amended) The method for performing a group-multiply-sum-and-add instruction according to claim [12] 17, wherein the instruction comprises a [fixed-point] floating-point arithmetic operation.

15. (Amended) A multiplier processing system for performing a group-convolve instruction, said system comprising:

means for partitioning each of a plurality of operands into a plurality of symbols, said operands having a first defined bit width and said symbols having a second defined bit width, said second defined bit width [of said symbols] being dynamically variable;

means for multiplying a selection of symbols of a first operand with a selection of symbols of a second operand, each of such multiplications producing a selected product, said

selection determined by the indices of the symbols within the first and second operand as to perform a convolution; and

means for adding [each product] a plurality of selected products so as to produce a [single scalar result, said scalar result capable of being represented by a bit width which is equal to or less than said first defined bit width of said operands without a reduction in the accuracy of said result] plurality of result symbols, said result symbols provided to a plurality of partitioned fields of a result operand.

16. (New) The method of claim 8, wherein said operands have a first bit width and said symbols have a second bit width, said second bit width being dynamically variable, and said scalar result is capable of being represented by a bit width which is equal to or less than said first defined bit width.

17. (New) The method of claim 12, wherein said operands have a first bit width and said symbols have a second bit width, said second bit width being dynamically variable, and said scalar result is capable of being represented by a bit width which is equal to or less than said first defined bit width.

18. (New) The multiplier processing system for performing a group-convolve instruction according to claim 15, wherein the instruction comprises a fixed-point arithmetic operation.

19. (New) The multiplier processing system for performing a group-convolve

instruction according to claim 15, wherein the instruction comprises a floating-point arithmetic operation.

20. (New) The multiplier processing system for performing a group-convolve instruction according to claim 15, wherein the summation-tree of the multiplier array is utilized in a close approximation to the manner required for a scalar multiply.

21. (New) The multiplier processing system for performing a group-convolve instruction according to claim 15, wherein the multiplier array required for a scalar multiply comprises an accumulation array partitioned to form a plurality of sums of products.

22. (New) A method for performing a group-multiply instruction in a general purpose, multiple precision parallel operation programmable media processor, said method comprising:

partitioning first and second registers into a plurality of floating point operands, said floating point operands having a defined bit width, wherein said defined bit width is dynamically variable;

multiplying, in parallel, said plurality of floating point operands in said first register by said plurality of floating point operands in said second, each of such multiplications producing a floating point product to provide a plurality of floating point products, each of said floating point products being capable of having a bit width which is equal to said predetermined bit width of said operands; and

providing said plurality of floating point products to a plurality of partitioned fields of a result.

23. (New) The method of claim 22 wherein each of said first and second registers are partitionable into four fields to hold four floating-point operands in parallel.

24. (New) The method of claim 22 wherein said first and second registers are 128 bit registers.

25. (New) The method of claim 22 wherein the result is returned to a result register which is a different register than either the first or second operand registers.

26. (New) A general purpose, multiple precision parallel operation programmable media processor for performing a group multiply instruction, said processor comprising:

first and second registers partitioned into a plurality of floating point operands, said floating point operands having a defined bit width and said defined bit width being dynamically variable;

a multiplier, configured to multiply, in parallel, said plurality of floating point operands in said first register by said plurality of floating point operands in said second register, each of such multiplications producing a floating point product to provide a plurality of floating point products, each of said floating point products being capable of having a bit width which is equal to said predetermined bit width of said operands; and

a result having a plurality of partitioned fields for receiving said plurality of floating point products.

27. (New) The processor of claim 26 wherein each of said first and second registers

are partitionable into four fields to hold four floating-point operands in parallel.

28. (New) The processor of claim 26 wherein said first and second registers are 128 bit registers.

29. (New) The processor of claim 26 further comprising a multiplier configured to group multiply a plurality of fixed point operands in parallel.

30. (New) The processor of claim 26 wherein the result is returned to a result register which is a different register than either the first or second operand registers.